Claims Appendix
(Showing Support for Claims)

1. Memory controller driver circuitry (FIG. 4, 400), comprising:

a data pad ([0059]; FIG. 4, DQ4);

N data propagation circuits (N≥2) ([0059]; FIG. 4, 402, 404);

a multiplexing stage ([0059]; FIG. 4, 406) which provides data to at least N-1 of the N data propagation circuits, said multiplexing stage enabling a coupling of a first data input stream (FIG. 4, 410) to each of the N data propagation circuits when the multiplexing stage is configured in a 1x mode, and said multiplexing stage enabling a coupling of different data input streams (FIG. 4, 410, 412) to various of the N data propagation circuits when the multiplexing stage is configured in an Mx mode (1<M≤N); and

output merging circuitry ([0059]; FIG. 4, 408) which alternately couples the N data propagation circuits to the data pad to thereby generate either a 1x or Mx stream of data bits at the data pad.

2. Memory controller driver circuitry (FIG. 8, 800) as in claim 1, further comprising:

a strobe pad ([0075]; FIG. 8, DQS18); and

means ([0075-0081]; FIG. 8, 824, 826, 828, 830, 832, 834) for producing at said strobe pad an Mx strobe signal which corresponds to said Mx data stream.

3. Memory controller driver circuitry as in claim 1, wherein said output merging circuitry comprises N sequentially clocked flip-flops ([0062]; FIG. 8, 808, 810) which respectively receive and output data from the N data propagation circuits.

4. Memory controller driver circuitry as in claim 1, wherein said output merging circuitry comprises a multiplexer which receives and sequentially outputs data from the N data propagation circuits ([0063]).

5. Memory controller driver circuitry as in claim 1, wherein said output merging circuitry comprises N tri-statable paths ([0062]; FIG. 5, 504, 506) which respectively receive and sequentially output data from the N data propagation circuits.

6. Memory controller driver circuitry as in claim 5, wherein each of said N tri-statable paths comprises one of N sequentially clocked flip-flops ([0062]; FIG. 5, 500, 502).

7. Memory controller driver circuitry as in claim 1, wherein N=M=2 (FIG. 4).

8. Memory controller driver circuitry as in claim 1, wherein a first of the N data propagation circuits is a simple wire route ([0072]; FIG. 8, 802).

9. Memory controller driver circuitry as in claim 1, wherein said data pad is a bidirectional data pad ([0114]).

10. - 16. (withdrawn)

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17. A computer system (FIG. 1, 124), comprising:

a CPU (FIG. 1, 102);

a memory controller ([0084]; FIG. 1, 100) coupled to said CPU;

an I/O controller (FIG. 1, 100) coupled to said CPU;

a number of I/O devices (FIG. 1, 112, 114, 116, 118, 120, 122) coupled to said I/O controller; and

a number of memory modules (FIG. 1, 104) coupled to said memory controller;

wherein said memory controller comprises a plurality of data pads ([0059]; FIG. 4, DQ4) to which is coupled data driver circuitry (FIG. 4, 400) for driving data to said memory modules; and

wherein said data driver circuitry comprises, for each data pad:

i) N data propagation circuits (N≥2) ([0059]; FIG. 4, 402, 404);

ii) a multiplexing stage ([0059]; FIG. 4, 406) which provides data to at least N-1 of the N data propagation circuits, said multiplexing stage enabling a coupling of a first data input stream (FIG. 4, 410) to each of the N data propagation circuits when the multiplexing stage is configured in a 1x mode, and said multiplexing stage enabling a coupling of different data input streams (FIG. 4, 410, 412) to various of the N data propagation circuits when the multiplexing stage is configured in an Mx mode (1<M≤N); and

iii) output merging circuitry ([0059]; FIG. 4, 408) which alternately couples the N data propagation circuits to the data pad to thereby generate either a 1x or Mx stream of data bits at the data pad.

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~~18~~. A computer system as in claim ~~17~~, wherein the memory controller further comprises a plurality of strobe pads ([0075]; FIG. 8, 800) to which is coupled strobe driver circuitry ([0075-0081]; FIG. 8, 824, 826, 828, 830, 832, 834) for driving strobes to said memory modules, said strobe driver circuitry comprising means for producing Mx strobe signals at said strobe pads.

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~~19~~. A computer system as in claim ~~17~~, wherein for each data pad, said output merging circuitry comprises N tri-statable paths ([0062]; FIG. 5, 504, 506) which respectively receive and sequentially output data from the N data propagation circuits.

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~~20~~. A computer system as in claim ~~17~~, wherein N=M=2 (FIG. 4).

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~~21~~. A computer system as in claim ~~17~~, wherein said memory controller and said I/O controller form an integrated memory and I/O controller (FIG. 1).